ABSTRACT OF THE DISCLOSURE

The present invention relates to a processor that performs a load operation prior to a store operation while avoiding ambiguous memory reference, and achieves high-speed operations. The present invention also relates to a method of controlling such a processor. This processor includes a history control unit that stores a storage destination of a result obtained by executing a second instruction that is executed prior to a first instruction placed before the second instruction. When it is determined that the address of first data to be processed by the first instruction is included in the address region of second data to be processed by the second instruction, the history control unit overwrites the result obtained by the execution of the first instruction on the second data corresponding to the address.